Vivian Brégier

✉ 18 rue du Bois Mentel,
38 400 Saint-Martin-d'Hères
☎ 09 51 82 04 51
06 64 70 29 23
✉ Vivian.Bregier@ens-lyon.org

EDA Software Engineer, PhD

Work experiences

since 2013 Software engineer at Mentor Graphics :
C++ development: implementation of new functionnalities, refactoring, and maintainance of calibre xL, TSV and xact-d extraction tools
infrastructure – Participation to Code Quality Initiative. The goal is to initiate background tasks to progressively improve the quality of the enormous codebase (10 million lines of code): common code, modularization, set up unit tests, measure tests coverage, going to c++11, ...

2007–2013 Analyst–developer at Atos Origin :
2012–203 **C++ development, integration and testing for ITER Organization**: fast acquisition for magnetic diagnostics
2009–2012 **C++ and ada developments** : nuclear reactor control software
2009 **Linux System** : Realization of a high availability radius server (software and hardware redundancy) for a satellite communication network for oil wells : sepecification, setup and validation
2008–2009 **C#.net development** : calibration software for electronic tools embedded inside drilling bits
2007–2008 **integration** of the components of an oil wells survey software, under Red Hat Linux

2003–2007 PhD at TIMA laboratory : *Automatic synthesis of optimized, proven quasi-delay-insensitive asynchronous circuits*

Skills

Software ingineering

Expert	C++(98,11,14)
Experienced	software design and architecture, unit testing, debugging, performance analysis
	C, python, ocaml, bash, LaTeX, xml, sql, ...
	Linux system (Debian, Red Hat)

EDA

General knowledge	netlist formats: spice, spef, dspf
	parasitic extraction

Languages

French	mother tongue
English	read, written, spoken fluently

Diploma

2007 PhD in microelectronics, INP Grenoble
2003 DÉA (equiv. Master) in computer science, ÉNS Lyon
2001 License in computer science, ÉNS Lyon
2000 License in Physics, ÉNS Lyon

Publications

[1] V. Brégier, B. Folco, L. Fesquet, and M. Renaudin. Modeling and synthesis of multi-rail multi-protocol qdi circuits. In *Thirteenth International Workshop on Logic and Synthesis*, 2004.

[2] B. Folco, V. Brégier, L. Fesquet, and M. Renaudin. Synthesis of area optimized quasi delay insensitive circuits. In *System On Chip 2005*, IFIP on VLSI, Perth, Austalia, 2005.

[3] B. Folco, V. Brégier, L. Fesquet, and M. Renaudin. *Technology Mapping for Area Optimized Quasi Delay Insensitive Circuits*, volume 200 of *IFIP Series*. Springer, 2006.